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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,871	05/17/2006	Kazuki Noda	59127US007	8302

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EXAMINER	
FORD, KENISHA V	

ART UNIT	PAPER NUMBER
2809	

NOTIFICATION DATE	DELIVERY MODE
09/10/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/595,871	NODA ET AL.	
	Examiner	Art Unit	
	Kenisha V. Ford	2809	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 11/06/2006.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1,3, 6,7,11** and **13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) in view of Miyakawa et al. (US 7,201,969 B2).

Regarding claim **1**, Wolk et al. discloses a method for manufacturing a semiconductor chip comprising:

- Applying a photothermal conversion layer, referred to as a light-to-heat conversion (LTHC) layer, that can convert light energy to heat energy (col. 2, lines 4-7). The LTHC disclosed comprises a light-absorbing agent (radiation absorber) that converts the radiation into heat to enable transfer of the transfer layer (heat decomposable resin) to the receptor (light-transmitting support) (col. 6, line 1-col 7, line 3).
- Preparing a semiconductor wafer by laminating the wafer, with a circuit face and photothermal conversion layer (or LTHC layer) facing each other, and irradiating light from the light-supporting side to cure the photocurable adhesive layer to have a non-circuit face on the outside (col. 9, lines 6-23; col. 10, lines 5-11 and 28-32)
- Irradiating radiation energy to decompose the LTHC layer (col. 7, lines 15-17)

Wolk et al. does not teach a method for grinding the non-circuit face of the wafer, dicing the ground semiconductor wafer, or optionally removing the adhesive layer from the semiconductor chips.

Miyakawa et al. discloses these limitations in its method of manufacturing a semiconductor chip comprising:

- Grinding the non-circuit face of the semiconductor wafer (col. 1, lines 30-34)
- Dicing the ground semiconductor wafer from the non-circuit face side to cut it into a plurality of semiconductor chips (col. 1, lines 34-35)
- Optionally removing the adhesive layer (col. 2, lines 31-48)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Miyakawa et al. in the device of Wolk et al. to produce a semiconductor wafer with an embedded integrated circuit that is then ground to the desired thickness and then diced to produce a plurality of semiconductor chips for use in hand-held information terminals, IC cards and the like (col. 3, lines 1-3).

Regarding claims **3**, Wolk et al. discloses a method for producing a semiconductor chip wherein the photothermal conversion layer, referred to as a light-to-heat conversion layer (LTHC), contains carbon black (col. 7, lines 27-33).

Regarding claims **6** and **11**, Wolk et al. does not teach a method for producing chip wherein the wafer is ground to a thickness of 50 μm or less.

However, Miyakawa et al. discloses that a semiconductor wafer can be ground or thinned until it is less than 200 μm and has been thinned to about 50 μm in some known cases (col. 3, lines 39-51).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Miyakawa et al in the device of Wolk et al. to produce a semiconductor chip with a thickness of 50 μm or less in order to meet the high demand for thinner semiconductor chips to be used in layered form (col. 3, lines 39-41).

Regarding claims **7** and **13**, Wolk et al. does not teach a method for producing a semiconductor chip wherein the photocurable adhesive layer has a storage modulus of $5x10^8$ Pa or more after curing.

However, Miyakawa et al. discloses that the storage elastic modulus of the base film, which is made of an adhesive layer (col. 6, lines 29-51), is between $5x10^8$ Pa to $1x10^{10}$ Pa (col. 7, lines 14-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Miyakawa et al in the device of Wolk et al. to produce a semiconductor chip with a photocurable adhesive layer that has a storage modulus of $5x10^8$ Pa or more after curing in order to have the strength to endure loads imposed in the direction of peeling during grinding (col. 6, lines 11-14).

3. Claims **2,4,8,12**,and **14-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) in view of Miyakawa et al. (US 7,201,969 B2) as applied to claim **1** above, and further in view of Oka (US 6,551,906 B2).

Wolk et al. and Miyakawa et al. fail to teach all limitations disclosed in claims 2,8 and 15-20.

Regarding claim **2**, Oka discloses the use of a die bonding tape, referred to as a protective tape, that is affixed to the semiconductor wafer before dicing the ground wafer (col. 1, lines 46-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Oka with those of Miyakawa et al. in the device of

Wolk et al. so that the wafer is diced in an adhered and secure condition in order to prevent the chips from being damaged during dicing.

Regarding claim **4**, Wolk et al. discloses a method for producing a semiconductor chip wherein the photothermal conversion layer, referred to as a light-to-heat conversion layer (LTHC), contains carbon black (col. 7, lines 27-33).

Regarding claims **8, 15-17** Oka discloses a method wherein the dicing of a semiconductor wafer is performed along scribe lines, also referred to as cutting grooves (col. 5, lines 35-44; col. 4, lines 13-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Oka with those of Miyakawa et al. in the device of Wolk et al. so that the wafer is precisely diced with the use of scribe lines.

Regarding claim **12**, Wolk et al. does not teach a method for producing chip wherein the wafer is ground to a thickness of 50 μm or less.

However, Miyakawa et al. discloses that a semiconductor wafer can be ground or thinned until it is less than 200 μm and has been thinned to about 50 μm in some known cases (col. 3, lines 39-51).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Miyakawa et al in the device of Wolk et al. to produce a semiconductor chip with a thickness of 50 μm or less in order to meet the high demand for thinner semiconductor chips to be used in layered form (col. 3, lines 39-41).

Regarding claim **14**, Wolk et al. does not teach a method for producing a semiconductor chip wherein the photocurable adhesive layer has a storage modulus of $5x10^8$ Pa or more after curing.

However, Miyakawa et al. discloses that the storage elastic modulus of the base film, which is made of an adhesive layer (col. 6, lines 29-51), is between $5x10^8$ Pa to $1x10^{10}$ Pa (col. 7, lines 14-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Miyakawa et al in the device of Wolk et al. to produce a semiconductor chip with a photocurable adhesive layer that has a storage modulus of $5x10^8$ Pa or more after curing in order to have the strength to endure loads imposed in the direction of peeling during grinding (col. 6, lines 11-14).

Regarding claim **18**, Oka discloses the use of a die bonding tape, referred to as protective tape, that is affixed to the semiconductor wafer before dicing (col. 1, lines 46-59) the ground wafer that Miyakawa et al. teaches that the wafer can be ground or thinned until it is about 50 μm (col. 3, lines 39-51).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Oka with those of Miyakawa et al. in the device of Wolk et al. so that the wafer that has been ground to about 50 μm is diced in an adhered and secure condition to prevent the chips from being damaged during dicing.

Regarding claim **19**, Oka discloses the use of a die bonding tape, referred to as protective tape, that is affixed to the semiconductor wafer before dicing (col. 1, lines 46-59) the ground wafer that Miyakawa et al. teaches can be ground or thinned until it is about 50 μm (col. 3, lines 39-51) and the storage modulus of the adhesive layer (col. 6, lines 29-51), is between $5x10^8$ Pa to $1x10^{10}$ Pa (col. 7, lines 14-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Oka with those of Miyakawa et al. in the device of Wolk et al. so that the wafer with an adhesive layer, with a storage modulus between $5x10^8$ Pa to

$1x10^{10}$ Pa, has been ground to about 50 μm having a dicing tape bonded to it so the wafer can be diced in an adhered and secure condition to prevent the chips from being damaged during dicing.

Regarding claim **20**, Oka discloses the use of a die bonding tape, referred to as a protective tape, that is affixed to the semiconductor wafer before dicing the ground wafer (col. 1, lines 46-59) and a method wherein the dicing of a semiconductor wafer is performed along scribe lines, also referred to as cutting grooves (col. 5, lines 35-44; col. 4, lines 13-20).

Oka does not teach that the wafer can be ground to 50 μm or less.

However, Miyakawa et al. does in fact teach that the wafer can be ground or thinned until it is about 50 μm (col. 3, lines 39-51).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Oka with those of Miyakawa et al. in the device of Wolk et al. so that the wafer that has been ground, to a thickness of 50 μm or less, is diced in an adhered and secure condition to prevent the chips from being damaged and so that the wafer is easily diced because of the scribing.

4. Claims **5** and **9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) in view of Miyakawa et al. (US 7,201,969 B2) as applied to claim **1** above, and further in view of d'Aragona et al. (US 4,818,323).

Wolk et al. and Miyakawa et al. fail to teach the limitation of laminating the semiconductor wafer in a vacuum as in claims **5** and **9**.

However, d'Aragona et al. discloses a method for producing a semiconductor chip wherein laminating the wafer is performed in a vacuum (col. 2, lines 45-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of d'Aragona et al. with those of Miyakawa et al. in the device of Wolk et al. to laminate a wafer in a vacuum to insure the device will be free of voids.

5. Claim **10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) in view of Miyakawa et al. (US 7,201,969 B2) and Oka et al. (US 6,551,906 B2) as applied to claim **4** above, and further in view of d'Aragona et al. (US 4,818,323).

Wolk et al., Miyakawa et al. and Oka fail to teach the limitation of laminating the semiconductor wafer in a vacuum as in claim **10**.

However, d'Aragona et al. discloses a method for producing a semiconductor chip wherein laminating the wafer is performed in a vacuum (col. 2, lines 45-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of d'Aragona et al. with those of Oka and Miyakawa et al. in the device of Wolk et al. to laminate the wafer in a vacuum to insure the device will be free of voids.

6. Claims **2, 18** and **19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) in view of Miyakawa et al. (US 7,201,969 B2) as applied to claim **1** above, and further in view of Fukuoka et al. (US 6,939,741 B2).

Wolk et al. and Miyakawa et al. fail to teach all limitations disclosed in claims 2,18 and 19.

Regarding claim **2**, Fukuoka et al. discloses the use of a die bonding tape, referred to as dicing tape, that is affixed to the semiconductor wafer before dicing the ground wafer (col. 1, lines 24-29 and col. 16, lines 43-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Fukuoka et al. with those of Miyakawa et al. in the device of Wolk et al. so that the wafer is diced in an adhered and secure condition in order to prevent the chips from being damaged during this process.

Regarding claim **18**, Fukuoka et al. discloses the use of a die bonding tape, referred to as dicing tape, that is affixed to the semiconductor wafer before dicing (col. 1, lines 24-29 and col. 16, lines 43-47) the ground wafer that Miyakawa et al. teaches that the wafer can be ground or thinned until it is about 50 μm (col. 3, lines 39-51).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Fukuoka et al. with those of Miyakawa et al. in the device of Wolk et al. so that the wafer that has been ground to about 50 μm is diced in an adhered and secure condition to prevent the chips from being damaged during this process.

Regarding claim **19**, Fukuoka et al. discloses the use of a die bonding tape, referred to as dicing tape, that is affixed to the semiconductor wafer before dicing (col. 1, lines 24-29 and col. 16, lines 43-47) the ground wafer that Miyakawa et al. teaches can be ground or thinned until it is about 50 μm (col. 3, lines 39-51) and the storage modulus of the adhesive layer (col. 6, lines 29-51), is between $5x10^8$ Pa to $1x10^{10}$ Pa (col. 7, lines 14-17).

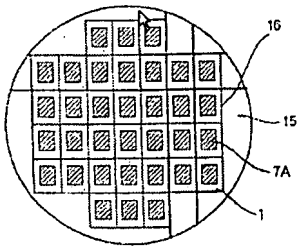
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Fukuoka et al. with those of Miyakawa et al. in the device of Wolk et al. so that the wafer with an adhesive layer, with a storage modulus between $5x10^8$ Pa to $1x10^{10}$ Pa, has been ground to about 50 μm having a dicing tape bonded to it so the wafer can be diced in an adhered and secure condition to prevent the chips from being damaged during the process.

7. Claims 8 and **15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) in view of Miyakawa et al. (US 7,201,969 B2) as applied to claim **1** above, and further in view of Uchida (US 6,620,649 B2).

Wolk et al. and Miyakawa et al. fail to teach the limitations of claims 8 and **15-17**.

However, Uchida discloses a method wherein the dicing of a semiconductor wafer (15) is performed along scribe lines (16) (fig. 2(*h*), col. 5, lines 23-30) and the alignment (col. 3, lines 1-16; col. 5, lines 27-31).

Fig. 2(h)



Reproduced from US 6,620,649 B2

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida with those of Miyakawa et al. in the device of Wolk et al. so that the wafer is precisely diced with the use of scribe lines.

8. Claims 8 and **15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) in view of Miyakawa et al. (US 7,201,969 B2) as applied to claim **1** above, and further in view of Morita et al. (US 5,414,297).

Wolk et al. and Miyakawa et al. fail to teach the limitations of claims 8 and **15-17**.

However, Morita et al. discloses a method wherein the dicing of a semiconductor wafer is performed along scribe lines (col. 3, lines 21-24; col. 5, lines 33-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Morita et al. with those of Miyakawa et al. in the device of Wolk et al. so that the wafer is that the wafer is precisely diced with the use of scribe lines.

9. Claim **20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolk et al. (US 6,214,520 B1) in view of Miyakawa et al. (US 7,201,969 B2) and Fukuoka et al. (US 6,939,741 B2) as applied to claim **2** above, and further in view of Uchida (US 6,620,649 B2).

Wolk et al. fails to teach the limitations of claim 20.

Fukuoka et al. discloses the use of a die bonding tape, referred to as dicing tape, that is affixed to the semiconductor wafer before dicing (col. 1, lines 24-29 and col. 16, lines 43-47) the ground wafer that Miyakawa et al. teaches can be ground or thinned until it is about 50 μm (col. 3, lines 39-51).

Fukuoka et al. and Miyakawa et al. do not teach a method wherein the dicing is performed while recognizing scribe lines and with alignment via light passing through the light-transmitting support and photothermal conversion layer.

However, Uchida does disclose a method wherein the dicing of a semiconductor wafer (15) is performed along scribe lines (16) (fig. 2(*b*), col. 5, lines 23-30) and the alignment (col. 3, lines 1-16; col. 5, lines 27-31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida with those of Miyakawa et al. and Fukuoka et al. in the device of Wolk et al. so that the wafer that has been ground to about 50 μm is diced in an adhered and secure condition to prevent the chips from being damaged and so that the wafer is that the wafer is precisely diced with the use of scribe lines.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenisha V. Ford whose telephone number is (571) 270-3328. The examiner can normally be reached on Monday-Thursday 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm Ullah can be reached on (571) 272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KVF

AKM ULLAH
SUPERVISORY PATENT EXAMINER